METHOD FOR PREPARING AND ASSEMBLING SUBSTRATES

Technical field and prior art

The invention relates to the field of assembling wafers or slices or layers of material, notably semiconductors, and of their preparation with the purpose of assembling them.

Among the assembly techniques of such substrates, molecular adhesion allows to assemble flat structures of low surface roughness.

It allows to obtain unique structures and is particularly well adapted for bonding together wafers of material used in microelectronics, such as, for example, wafers in silicon, or III-V material (AsGa, InP) or glass or fused silica glass substrates.

Nowadays this technique is used industrially, for example in the manufacture of SOI (Silicon On Insulator) material.

The known methods for manufacturing SOI material, which use molecular adhesion, implement two wafers 2, 4 of silicon (figure 1, part A), of which at least one of the two has a layer 6 of oxide on the surface.

These two wafers are of standard size. The edges 5 and 7 are generally chamfered, so as to avoid fractures likely to appear during eventual manufacturing of components or in the event of shocks to still sharp edges. There are rounded and/or bevelled chamfers. Figure 2 represents, in greater detail, an example of a chamfer zone 5, of width L (measured on a plane parallel to the mean plane P of the wafer) of a wafer 4, of thickness e.

The assembling firstly comprises a surface preparation stage, a putting together stage (figure 1, part B), generally followed by a heat treatment stage.

Normally, this heat treatment is performed at 1100°C for 2 hours for SOI substrates.

Then, as illustrated in figure 1, part C, at least one of the two wafers is thinned out via surface edge grinding and/or mechanical polishing and/or mechano-chemical polishing.

The chamfers 5 and 7 generate the existence of a non-bonded zone on the wafer edges.

After thinning out, a membrane 8 made in silicon remains bonded to the centre, but detached on the edges, as visible in figure 1, part C.

The detached edge of the membrane must be removed, as it is likely to break in an uncontrolled manner and introduce particles on the other surfaces, and notably on surface 9 of the membrane 8, or on components made in the membrane 8.

For this reason a stage for routing or eliminating matter in the peripheral zone is performed in order to

eliminate this edge zone from the membrane 8, as illustrated in figure 1, part D.

This routing is normally performed via mechanical means.

This stage is very delicate. For example, in the event of mechanical machining, it is difficult to trim everything and to stop exactly at the bonding interface, which in this case is the upper surface of the oxide layer 6. Indeed, either we stop just above this interface leaving some matter above the latter, or we stop in the support 2 and the surface polish of the edges of the front face of the support is lost.

It is therefore important to find a means of properly and accurately trimming a wafer of material.

This phenomenon is also important in the case where at least one of the two wafers contains all or part of an electronic or opto-electronic device, or a micro-system, or a nano-system or another component.

The same problem exists if the assembling of the two wafers is done via bonding instead of molecular adhesion, or even without the oxide layer 6 on the surface of the wafer 12.

PRESENTATION OF THE INVENTION

The invention firstly relates to a method for assembling a first and a second wafer of material, comprising:

- a trimming stage of at least the first wafer;
- an assembling stage of at least the first wafer, trimmed, and of the second wafer.

According to the invention, a machining, or trimming or eliminating stage of the matter in a peripheral section of at least the first wafer, is thus performed before bonding or assembling the two wafers together.

A thinning out stage of at least the first wafer can then be carried out, leaving a layer on the second wafer. A transplanting or transferring of this layer is thus achieved.

The invention also relates to a method for transplanting or transferring a layer of material, circuits or components, known as transplant or transfer layer, comprising:

- the trimming of a first wafer of material, or the elimination of matter in a peripheral section of a first wafer, in which the layer to transfer is made, at least in a zone located around or on the periphery of this layer to transfer;
- the transplanting or transferring of this layer onto a second wafer of material.

This transplanting or transferring is performed via assembling the first and second wafers and then thinning out the first wafer.

The first wafer of the method for assembling, transplanting or transferring is for example a chamfered wafer, bearing at least one chamfered edge. The trimming thus relates to at least a part of the chamfered edge. It can also eat into a part, notably peripheral, of the transplant or transfer layer.

The method for assembling or transplanting according to the invention thus allows to obtain a

structure with a first wafer, possibly chamfered, perfectly trimmed before assembling, the trimming being devoid of the problems developed above in the context of the prior art, problems due to the existence of a second wafer.

It can apply as much to wafers containing all or part of an electronic component or other, as to blank wafers, such as wafers known as "bulk".

Trimming stages before assembling can be performed before or after possible surface preparation stages with the purpose of assembling or transplanting.

The first wafer can be routed or trimmed through its entire thickness, or through a lesser thickness, for example equal to or greater than the final thickness of the layer that is sought after or transplanted onto the second wafer.

According to an alternative, the trimming can also be performed over a thickness that is less than this final thickness.

In this case, it could be beneficial to end the routing, in a standard manner, after assembling, with one or other of the two faces of the first wafer.

If the substrates or wafers have comparable initial dimensions or initial diameters, the thickness of the trimming can be such that the routed wafer has, after trimming, a dimension or diameter less than the other wafer.

Preferably, in the case where the first wafer has a rollover edge or chamfer, the width, measured on the plane of the wafer, on which the upper wafer is trimmed,

is greater than or equal to the width of the rollover or chamfer.

It can also have a width greater than or equal to the width of the zone which can not be bonded or assembled due to the rollover or chamfer.

The first wafer can have a zone or a cleavage or fracture plane, created in depth for example by hydrogen implantation or by the creation of a buried porous zone or by the creation of a removable bonding interface.

When the thickness of the routed zone is greater than the thickness of the desired thin layer, this routed wafer can be recycled, without the need of routing before bonding onto a new substrate. A new fracture plane can thus be created, then it can be directly assembled with a new substrate.

The assembling of the two wafers can be performed via molecular adhesion or via bonding, through the adding of matter such as for example adhesive or wax.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1, parts A-D, represents stages of a known method for assembling substrates.

Figure 2 represents a part of a substrate and its edge or rollover edge.

Figure 3, parts A-D, represents stages of a method according to the invention.

Figures 4, parts A-C, and 5, parts A-B, represent an alternative of a method according to the invention.

Figure 6, parts A-D, represents an alternative of a method according to the invention, in the case of a substrate with a weakened plane.

Figure 7, parts A-D, represents an alternative of a method according to the invention, in the case of a substrate with a protective or bonding layer.

Figures 8A-8D represent a front view of the routed or trimmed wafers.

Figure 9 represents a wafer of material with a lateral shoulder.

EXAMPLES OF EMBODIMENTS OF THE INVENTION

Figure 3, parts A-D, represents stages of a method according to the invention.

Two wafers 12 and 14 are chosen, for example two wafers of semiconductor material, such as standard silicon wafers.

These wafers can typically have a thickness of between 300 µm and 800 µm. They are for example wafers of 100 mm or 200 mm or 300 mm in diameter.

For the aforementioned reasons, the edges 15 and 17 are chamfered.

Components or circuits 16 may have previously been made in the wafer 12, but the invention also relates to the case of a wafer 12 absent of any circuit, the reference 16 thus designating a layer of material to be transferred onto the wafer 14. In figure 3, part B, the surface of this layer 16 of circuits or material to be transplanted or transferred lies flush with the surface of the wafer 12.

A routing or matter eliminating stage is then performed (figure 3, part B), starting from the face 19 of the wafer 12 to be assembled with the wafer 14, over a thickness ed and a width Ld.

The width Ld is measured on a plane parallel to the mean plane of the wafer. This stage, performed before the assembling or transplanting stage onto the wafer 14, allows to eliminate, at least partially and from the assembly face 19, the matter located in the peripheral zone, or located around the transplant layer 16, zone which is likely to have problems caused by the non-bonded edges.

Ld is preferably greater than or equal to the width L of the rollover edge or the chamfer (figure 2). It can be from about a few hundred µm to a few mm, for example of between 100 µm and 5 mm.

Ld is notably greater than L in the case where the non-bonding zone or zone which can not adhere to a substrate after assembling, as illustrated in stage C of figure 1, is itself greater than L.

Indeed, this "non-bonding" or "non-assembling" zone depends on the manner the rollover edge is made on the wafer 12 but also on the wafer 14.

It can also depend on the technical stages that could have been previously performed on the upper wafer 12 and on the support wafer 14. Regarding the width L, some stages can increase the width of this non-bonded zone (for example oxidising or depositing stages), others can reduce this said width (for example a levelling or flattening or polishing stage).

Ld can therefore be greater than or equal to the width of this non-bonding or non-assembling zone.

The thickness ed will be less than the thickness e of the wafer. It can be substantially equal to or greater or lesser than the thickness of the layer 16 (stage D, figure 3) or of the membrane to be obtained after the future thinning out or transplanting stage onto the wafer 14.

By way of example ed can be about a few µm or between 1 µm (or 10 µm) and 100 µm or even between 5 µm and 60 µm. As for the layer 16, it can have a thickness, for example, between 1 µm and 60 µm.

If ed is less than the thickness of the layer 16 (stage D, figure 3) or of the membrane to be obtained after the future thinning out or transplanting stage, then the assembling stage can be followed by an additional trimming of the remaining section of substrate 12, as will be explained below.

The trimming stage before assembling can be performed in a mechanical and/or chemical (notably humid) and/or via plasma and/or in a mechano-chemical manner. The mechanic routing can be performed for example via "edge grinding" or "edge polishing".

It then proceeds with the assembling of the two wafers (stage C, figure 3) for example via molecular adhesion.

As explained above, the assembling comprises for example a surface preparation stage, a putting into contact stage and a heat treatment stage.

This heat treatment stage is performed at a few hundred degrees Celsius, for example between 100 and

1200°C, or even 1100°C, and this for a time span from a few minutes to a few hours, for example between 10 minutes and 3 hours, or even 2 hours.

Then, as illustrated in figure 3 (stage D), at least one of the two wafers is thinned down to the desired thickness, for example over a thickness greater than or equal to e-ed, via edge grinding and/or mechanical polishing and/or mechano-chemical polishing and/or chemical polishing. In figure 3 (stage D), the thinned wafer is the previously routed wafer 13.

After thinning out of the latter, a membrane made in semiconductor material, or even the layer 16 of components or circuits, thus remains bonded or assembled to the wafer 14, towards its centre. There are no lateral membranes nor any non-bonded lateral residue. The transplanting or transferring of the layer 16 is thus better than with the technology of the prior art.

Figure 4, part A, corresponds to the aforementioned case where the depth ed over which the wafer 12 was routed before assembling is insufficient to completely remove the layer 16 during the thinning out stage.

Assembling, which has led to the structure of figure 4, part A, can thus be followed with an additional trimming, from the edges 13 located on the side of the front face or from the assembling face, in order to obtain a routed zone over a thickness ed greater than that of the layer 16 (figure 4, part B).

It is also possible to perform this additional trimming from the edges 21 located on the rear face, opposite the assembling face.

This additional trimming stage is free of the problems disclosed in the introduction to this application: there is notably no risk of etching out the substrate 14. It can then be followed by the thinning out stage of the substrate 12, as described above (figure 4, part C).

Here again we obtain a transplant or a transfer free of membrane or lateral residue.

According to an alternative, the wafer 12 is completely routed over its entire thickness (figure 5, part A). This is the case where ed=e.

The assembling stage leads to the device represented in figure 5, part B, which can then be thinned out as explained above.

The wafer 12 then has a width or diameter less than that of the wafer 14.

As illustrated in figure 6, part A, the invention also applies to an initial substrate 22 in which a weakened plane 26 was made, for example via previous ion implantation (for example a hydrogen implantation) or via creating a buried porous zone, as explained for example in the document by S.S.Iyer and al. "Silicon wafer bonding technology for VLST and MEMS applications", published by INSPEC, 2002, Antony Rowe Ltd, or via creating a removable bonding interface.

It then proceeds with the trimming of this substrate (figure 6, part B) over a part of its thickness or over all of its thickness, as explained

above, then with the assembling of the two substrates 22 and 24.

For example, a heat treatment allows to separate the substrate 22 at the ion implantation layer 26 of hydrogen ions (figure 6, part D).

This results, on one hand in a unit made of the substrate 24 with a superficial layer 28 of material which comes from the initial substrate 22, and on the other hand in a substrate 23 which also comes from the initial substrate 22 and which is reusable for subsequent operations. If the thickness over which the substrate 22 was trimmed is greater than the thickness of the transplant layer 28, this substrate 22 can notably be subjected to a new ion or atom implantation, then a new transferring or transplanting stage after assembling with a new substrate 24, but without the need to perform a new trimming stage.

The invention, such as is described above in connection with one of the figures 3-6, also applies in the case where the initial substrate 12 and 22 has the shape illustrated in figure 9, with a shoulder 25 on the edges of the wafer.

These shoulders define a stiffening located at a depth P, for example lying between 50 nm and 2 µm.

The routing stage allows to remove these shoulders.

An ion implantation stage, for the creating of a weakened plane 26, can take place before or after this trimming stage: a wafer is thus obtained which is identical to the one represented in part B of figure 6. The following stages in figure 6 can thus be performed as described above.

BSOI or thick SOI type structures can also be created in an efficient manner. The thinning out stage is then mechanic and/or mechano-chemical.

According to another example, electronic components are made in a wafer such as the wafer 12 (figure 3A) over a superficial thickness, for example, between 1 and 10 µm.

We trim via "surface edge grinding" the edge of the wafer over a thickness ed of 50 µm and along a width Ld of 3 mm.

This routing stage can be performed before surface preparation (for example via mechano-chemical levelling followed by chemical cleaning) and in order to reduce the number of cleansings before assembling.

Then the routed wafer (comprising the components) is bonded via molecular adhesion onto the support wafer. The structure is then annealed for example at a temperature of 300°C and for a time span of between a few minutes and a few hours.

The superficial wafer is then thinned out via surface edge grinding and mechano-chemical (figure 3, part D) and/or chemical polishing until a thickness de is obtained, for example, 10 µm.

A transplanted layer, comprising the components, transferred onto a support wafer is thus obtained.

According to another embodiment, the wafer 12 comprises components 16 and is covered on its surface with a protective layer 18, for example an oxide layer 18 (figure 7, part A). This can also be a bonding layer.

A crown 20 is defined via lithography which will correspond to the routing zone. A local chemical

etching allows to eliminate, on this zone, the protective layer 18 (figure 7, part B).

The edge of the substrate 12 is then etched (figure 7, part C), for example via chemical (ex. TMAH) or plasma etching.

The wafer is then cleaned, for example via chemical cleaning. According to an alternative, the cleaning is integrated into the chemical etching.

It can then proceed with the assembling on a wafer 14 as explained above (figure 7, part D).

Figures 8A-8D each represent a front view of a wafer 40 and 42 with a layer 41 and 43 of material around which routing was performed. This layer 41 and 43 is intended to be transplanted onto a second wafer, according to any one of the aforementioned embodiments. In figure 8A the wafer has a flattered zone 44.

Generally, the invention has the advantage of being able to be integrated into a method for manufacturing. This is notably the case when components are previously made in the wafers.

The invention also applies in the case of non-chamfered wafers, a stage for trimming or eliminating matter in a peripheral zone of one of these two wafers being nonetheless performed before assembling the two wafers. The other processing stages are similar to those described according to one or other of the embodiments described above or below.

The method set forth in the invention is also well suited to the manufacturing of BSOI type material, or even to the transplanting of a layer of III-V material onto silicon for example.

In the case of BSOI a wafer of silicon is first oxidised in order to obtain a layer of silicon dioxide, which will serve as buried oxide.

This wafer is then routed over a 1.5 mm wide zone which corresponds to the rollover edge of the wafer, as explained above.

The surface of the wafer is then cleaned, for example via chemical and/or mechano-chemical cleaning stages.

Its surface is bonded via molecular adhesion onto a second wafer, made in silicon, and the unit is annealed at 1100°C for 2 hours.

A surface edge grinding stage followed by a mechano-chemical polishing allows to thin the wafer down to the desired thickness in order to obtain the SOI substrate.

This said method can apply to the transplanting of III-V material such as AsGa or InP onto another material such as a semiconductor notably silicon.

This said method can also apply to the transplanting of semiconductor material such as Germanium or Germanium silicon (SiGe) onto a substrate made in another material such as a semiconductor, notably silicon.

Likewise, this method can be used to perform a transplanting of wafers of non-semiconductor material, for example wafers of insulating material such as glass or quartz, or piezoelectric material such as LiNbO3 or LiTaO3, which allows to obtain a perfectly routed thin film on a support of the same nature or of a different

nature, for example a semiconductor substrate and notably silicon.

The wafers of material prepared and assembled according to the invention are wafers of "bulk" material.

CLAIMS

1. Method for assembling a first and a second wafer (12, 14, 22, 24), of which at least the first, known as chamfered wafer, has at least a chamfered edge (7, 17), comprising:

- a routing stage of at least one part of the chamfered edge of the first wafer (12, 22);
- then, an assembling stage of the first wafer, routed, and of the second wafer.

2. Method as in claim 1, further comprising, after assembling, a thinning out stage of at least the first wafer, leaving at least a layer (16) on the second wafer.

3. Method for transplanting a layer (16, 28) of material or circuits or components, known as transplant layer, comprising:

- the routing of a first wafer (12, 22) of material, in which the transplant layer is made, at least around or on the periphery of this transplant layer;
- the transplanting of this layer onto a second wafer (14, 24) of material.

4. Method as in claim 3, in which a part of the material of the transplant layer is eliminated during routing.

5. Method as in one of claims 1 to 4, the routing stage being performed over the entire thickness e of the first wafer.

6. Method as in one of claims 1 to 4, the routing stage being performed over a thickness ed less than the thickness e of the first wafer.

7. Method as in claim 6, the routing stage being performed over a thickness ed greater than or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted onto the second wafer.

8. Method as in claim 6, the routing stage being performed over a thickness ed less or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted onto the second wafer.

9. Method as in one of claims 1 to 8, comprising an additional routing stage after assembling the first and second wafers.

10. Method as in one of claims 1 to 9, the routing stage being performed over a thickness ed of the first wafer of between 1 µm and 100 µm.

11. Method as in one of claims 1 to 10, the fist wafer being chamfered and comprising at least a chamfered edge (5).

12. Method as in claim 11, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width L of the chamfered edge, measured on the same plane.

13. Method as in any of claims 1 to 12, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width of the zone of this first wafer which can not, without routing, be assembled with the second wafer.

14. Method as in any of claims 1 to 13, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer of between 100 µm and 5 mm.

15. Method as in any of the previous claims, the first wafer having a weakened plane (26) defining a thin layer in the wafer.

16. Method as in the previous claim, the first wafer being routed over a thickness greater than that of the thin layer.

17. Method as in claim 16, followed by:

- a thinning out stage via separation of the first wafer along the weakened plane, so as to leave the thin layer on the second wafer and leave a free portion (23) of the first substrate;
- a new creating stage of a new weakened plane in the portion (23) that remained free of the first substrate;
- an assembling stage of this portion (23) with a third substrate.

18. Method as in any of claims 15 to 17, the weakened plane being performed via ion implantation or via the creating of a buried porous zone or via the creating of a removable bonding interface.

19. Method as in any of claims 1 to 18, the first wafer comprising a lateral shoulder (25), eliminated during the routing stage.

20. Method as in any of claims 1 to 19, the assembling of the two substrates being performed via molecular adhesion or via bonding using an adhesive substance.

21. Method as in any of the previous claims, components or circuits (16) having been made in the first wafer before routing.

22. Method as in any of the previous claims, the first wafer previously being covered in a protective layer (18).

23. Method as in the previous claim, the protective layer being eliminated locally, before routing of the first wafer, in a zone located above the zone to be routed of the first wafer.

24. Method as in the previous claim, the local elimination of the protective layer being performed via lithography and etching.

25. Method as in any of the previous claims, the routing taking place after a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

26. Method as in any of claims 1 to 24, the routing taking place before a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

27. Method as in any of the previous claims, the routing being performed via mechanical or chemical or mechano-chemical etching or via plasma etching or via a combination of at least two of these types of etching.

28. Method as in any of the previous claims, at least one of the two wafers being made in a semiconductor material.

29. Method as in the previous claim, at least one of the two wafers being made in silicon or in a III-V type semiconductor material.

30. Method as in any of claims 1 to 27, at least one of the two wafers being made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

ABSTRACT OF THE DISCLOSURE

The invention relates to a method for assembling a first and a second wafer (12 and 14) of material, comprising:

- a routing stage of at least the first wafer (12);
- an assembling stage of the first and the second wafer.

FIGURES 3A-3D.